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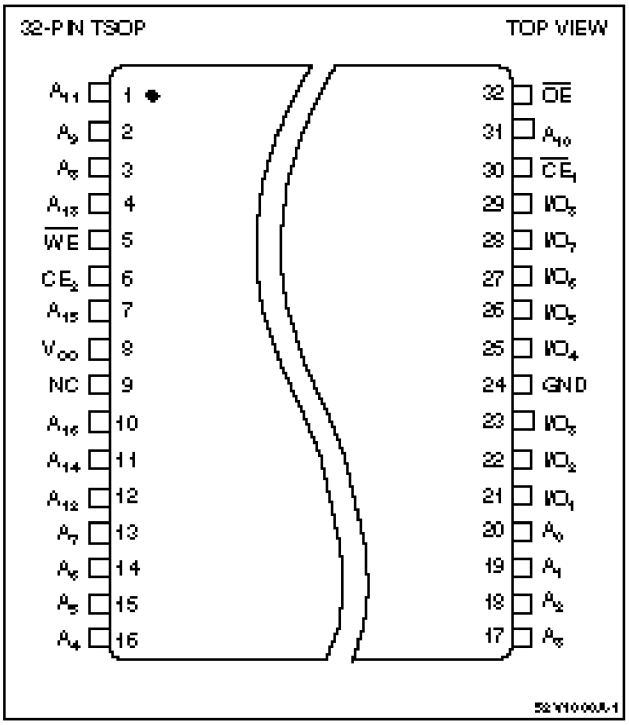
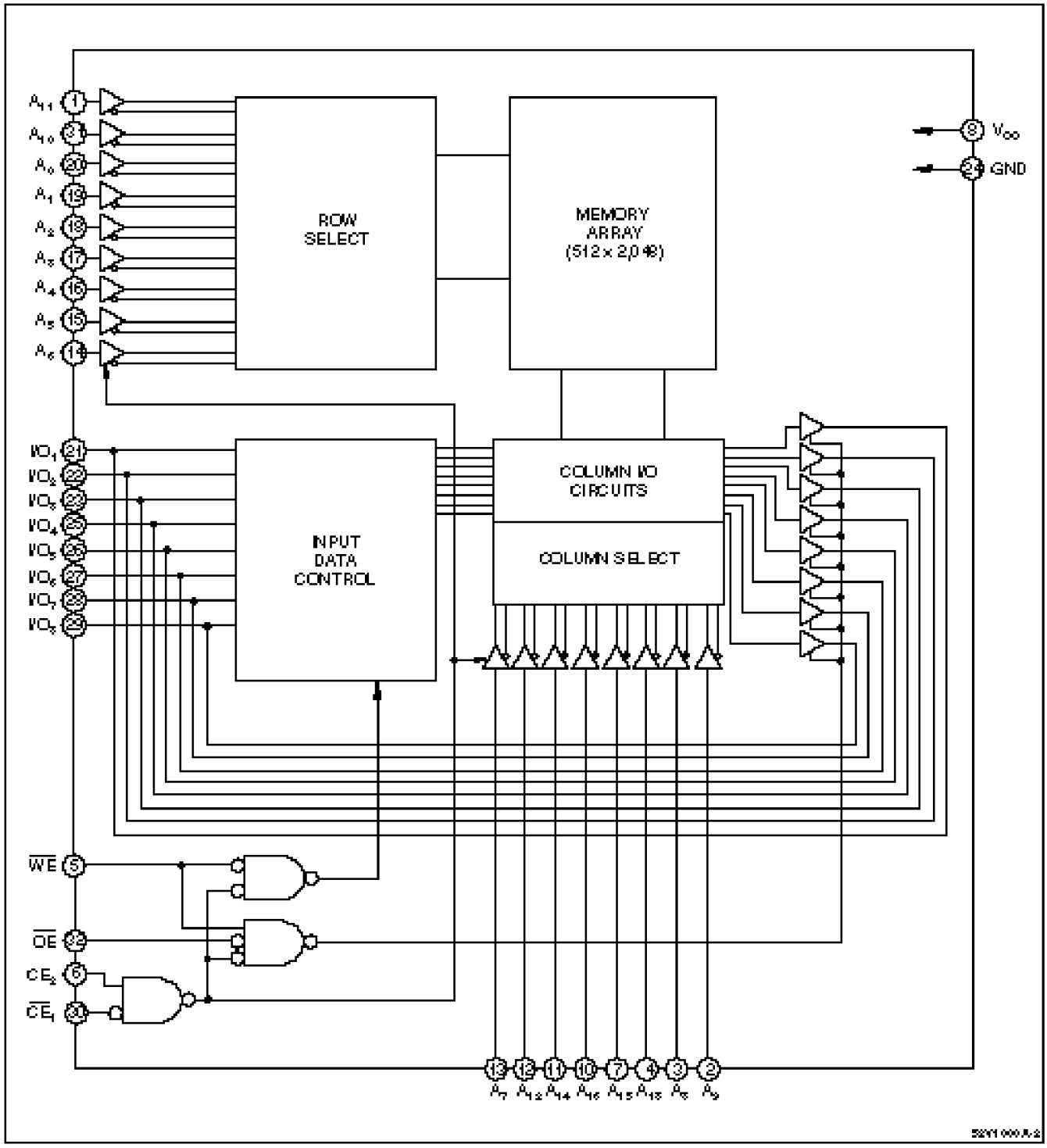

32-PIN TSOP
TOP VIEW
A11 1
A9 2
A8 3
A13 4
WE 5
CE2 6
A15 7
VCC 8
NC 9
A16 10
A14 11
A12 12
A7 13
A6 14
A5 15
A4 16
32 OE
31 A10
30 CE1
29 I/O8
28 I/O7
27 I/O6
26 I/O5
25 I/O4
24 GND
23 I/O3
22 I/O2
21 I/O1
20 A0
19 A1
18 A2
17 A3


ROW SELECT
MEMORY ARRAY (512 × 2,048)
COLUMN I/O CIRCUITS
COLUMN SELECT
INPUT DATA CONTROL
V_{CC}
GND
$\overline{WE}$
$\overline{OE}$
CE_2
$\overline{CE_1}$

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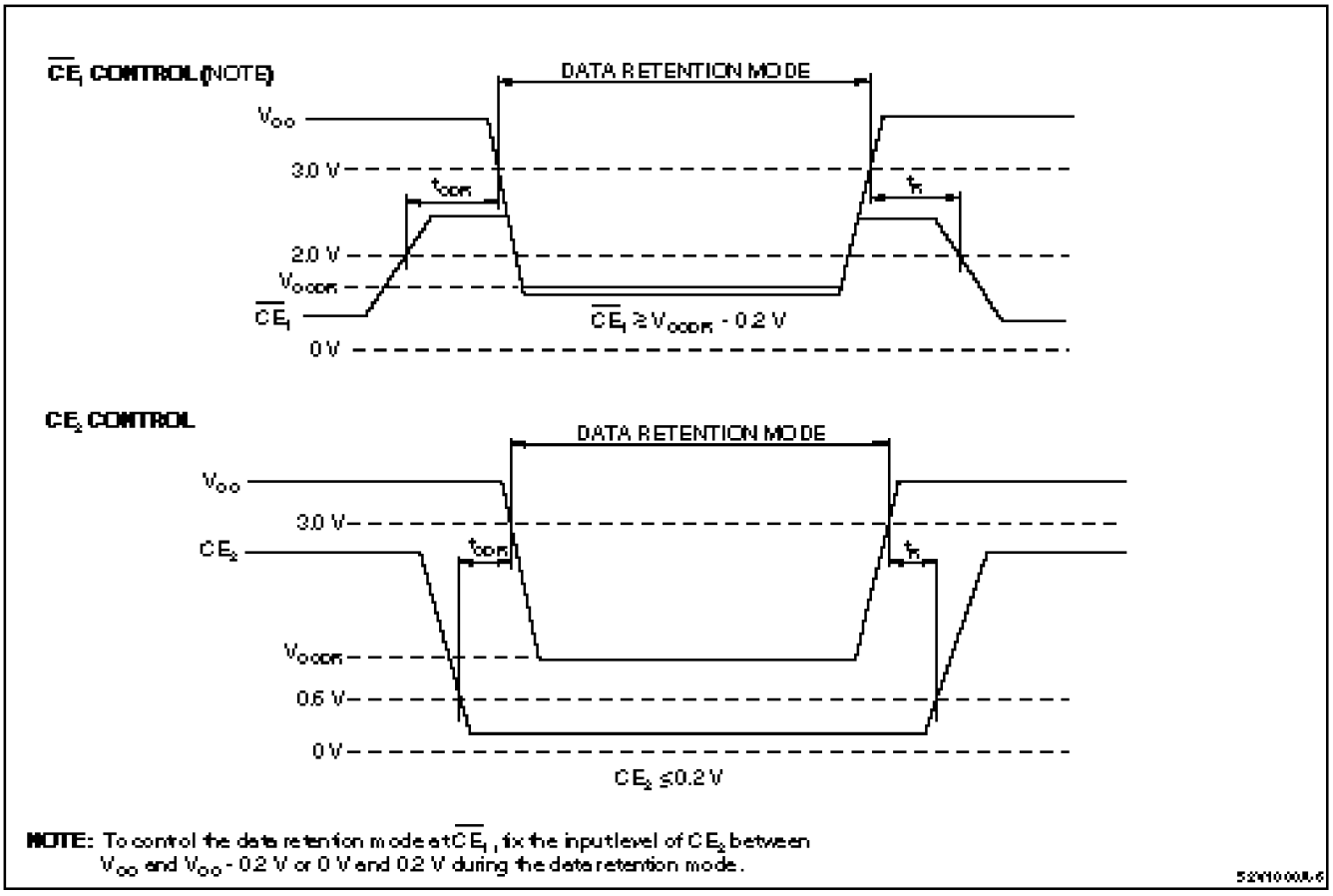
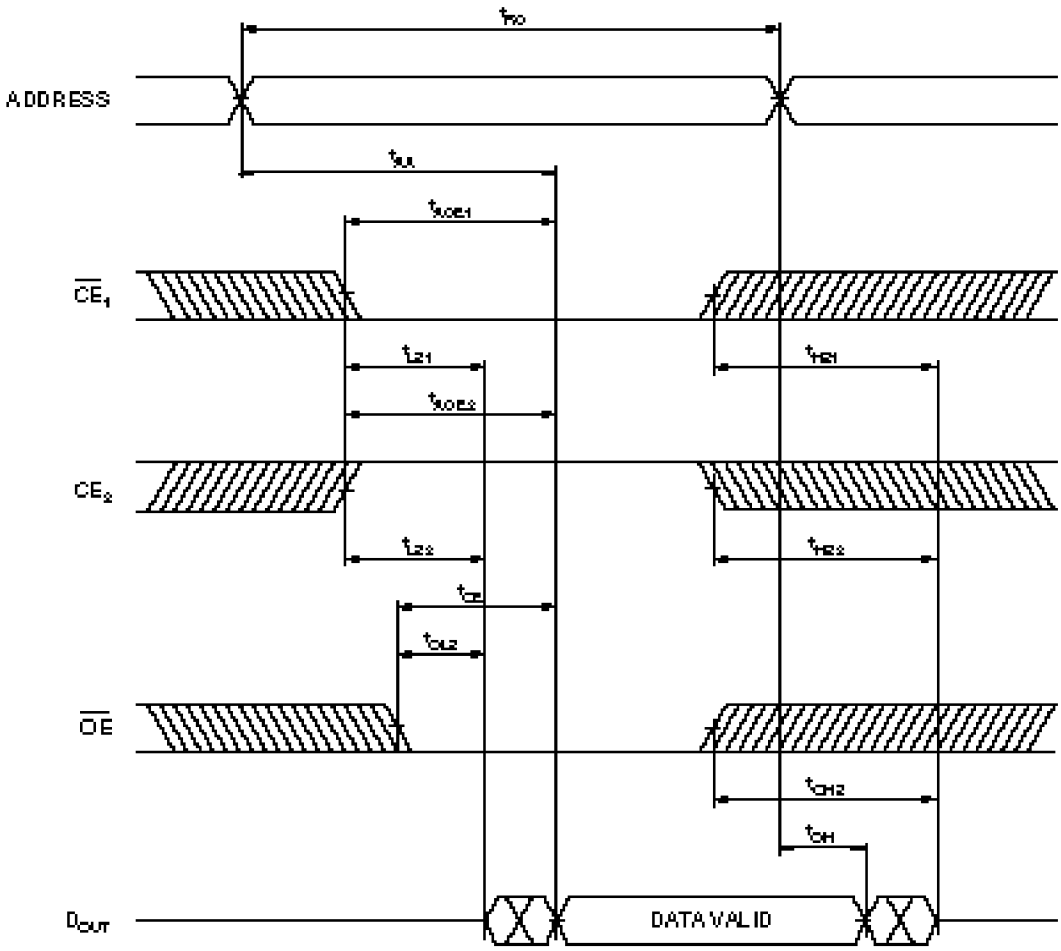
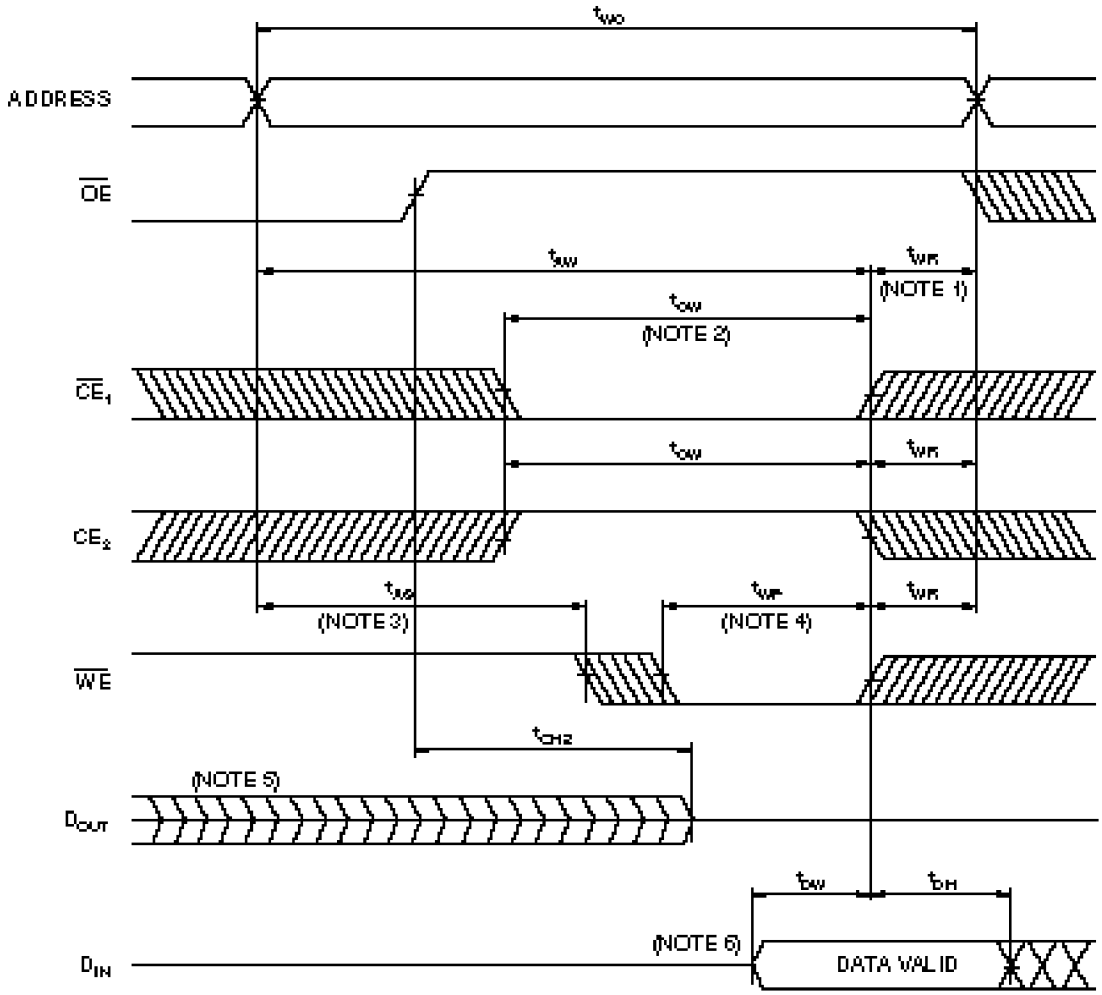

CE1 CONTROL (NOTE)
DATA RETENTION MODE
VCC
3.0 V
tCDR
tR
2.0 V
VCCDR
CE1
CE1 ≥ VCCDR - 0.2 V
0 V
CE2 CONTROL
DATA RETENTION MODE
VCC
3.0 V
CE2
tCDR
tR
VCCDR
0.6 V
0 V
CE2 ≤0.2 V
NOTE: To control the data retention mode at CE1, fix the input level of CE2 between VCC and VCC - 0.2 V or 0 V and 0.2 V during the data retention mode.



NOTE: $\overline{WE}$ is 'HIGH' level during the read cycle.



NOTES:

1. t_{WR} is defined as the time from writing finish to address change.
2. t_{CW} is defined as the time from the last occurring transition, either $\overline{CE_1}$ LOW transition or CE_2 HIGH transition, to the time when the writing is finished.
3. t_{AS} is defined as the time from address change to writing start.
4. The writing occurs during an overlapping period of $\overline{CE_1}$ = 'LOW', CE_2 = 'HIGH,' and $\overline{WE}$ = 'LOW' (t_{WP}).
5. If $\overline{CE_1}$ LOW transition or CE_2 HIGH transition occurs at the same time or after $\overline{WE}$ LOW transition, the outputs will remain high-impedance.
6. When I/O pins are in the output state, input signals with the opposite logic level must not be applied.

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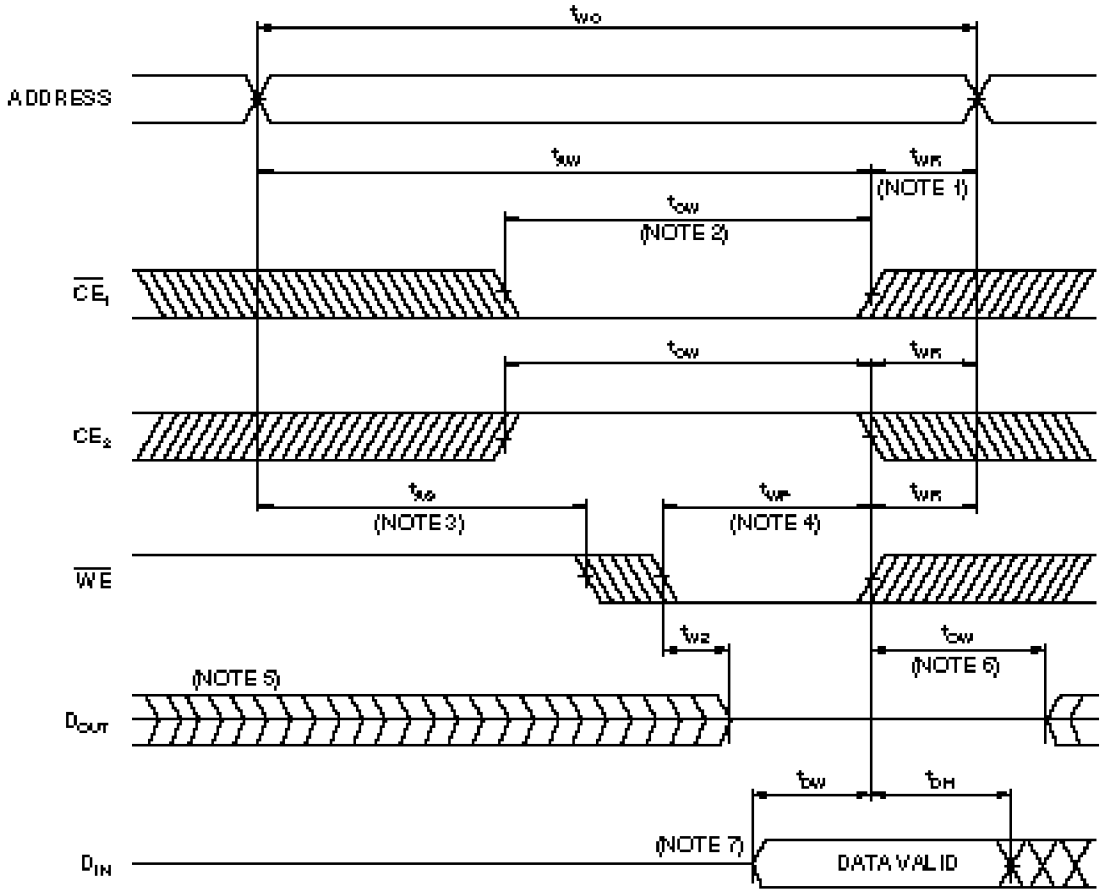

NOTES:

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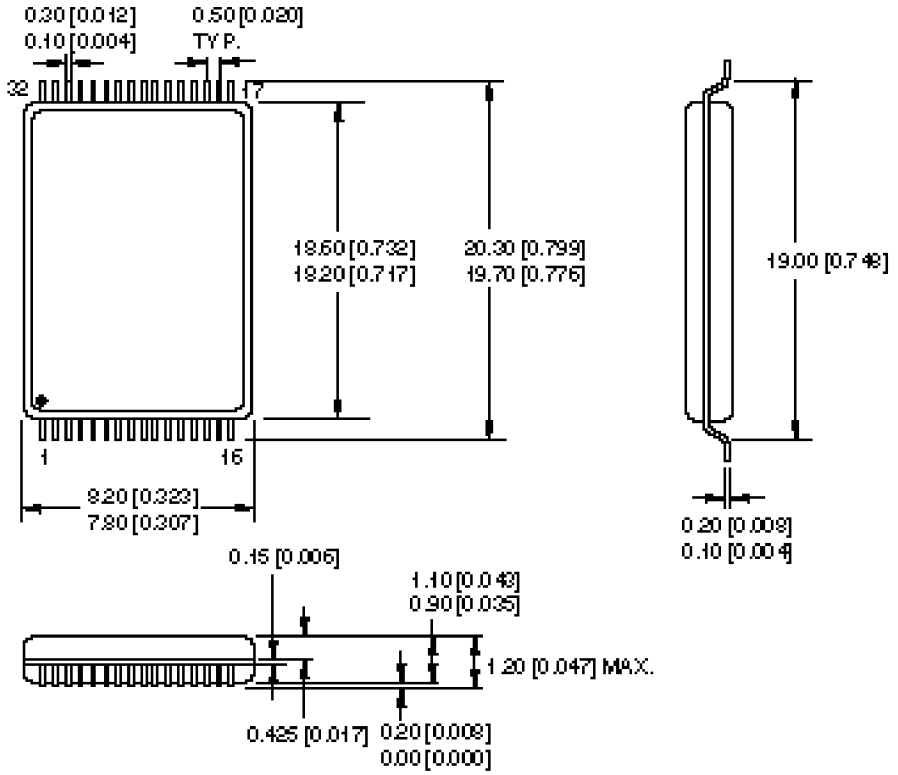
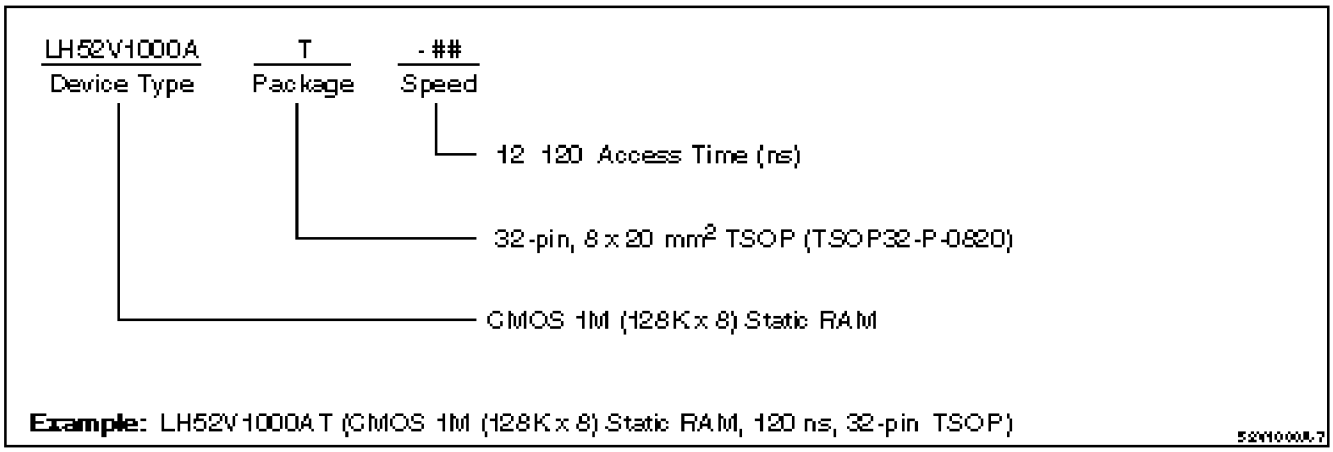
6. If $\overline{CE_1}$ HIGH transition or CE_2 LOW transition occurs at the same time or before $\overline{WE}$ HIGH transition, the outputs will remain high-impedance.
7. When I/O pins are in the output state, input signals with the opposite logic level must not be applied.

32TSOP (Type I) (TSOP032-P-0820)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

32TSOP



Example: LH52V1000AT (CMOS 1M (128K x 8) Static RAM, 120 ns, 32-pin TSOP)

52V1000A-7